Claims

What is claimed is:

1. A method for booting a host adapter device devoid of dedicated non-volatile program memory, wherein said host adapter device is associated with a motherboard having BIOS code stored in a non-volatile memory, said method comprising the steps of:

retrieving operational programmed instructions for said host adapter device from said non-volatile memory device of said motherboard;

downloading said operational programmed instructions from said motherboard to a volatile memory associated with said host adapter device; and

commencing operation of said host adapter device executing said operational programmed instructions to thereby boot said host adapter device.

2. The method of claim 1 further comprising the steps of:

retrieving data associated with said operational programmed instructions from said non-volatile memory device; and

downloading said data from said motherboard to said volatile memory.

3. The method of claim 1 wherein said host adapter device is coupled to said motherboard via a PCI bus and wherein the step of downloading comprises the steps of:

forcing said host adapter device into a diagnostic mode via said PCI bus; and

writing said operational programmed instructions into said volatile memory using direct memory access by said motherboard to said volatile memory via said PCI bus, and

wherein the step of commencing includes the step of:

releasing said host adapter device from said diagnostic mode via said PCI bus.

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4. The method of claim 3

wherein the step of forcing comprises the steps of:

setting a PreventIopBoot bit in a Host Diagnostic Register of said host adapter device;

setting a ResetAdapter bit in the Host Diagnostic Register;

awaiting clearing of the ResetAdapter bit in the Host Diagnostic Register; and

setting a DiagRwEn bit in the Host Diagnostic Register.

5. The method of claim 3

wherein the step of releasing further comprises the steps of:

writing an IopResetVectorRegAddr for operation of said operational programmed instructions in a DiagRw Address register of said adapter device;

writing an IopResetVectorValue for operation of said operational programmed instructions in a DiagRw Data register of said adapter device;

clearing the PreventIopBoot bit in the Host Diagnostic Register; and

writing any byte value in a Write Sequence Key field in a Write Sequence register of said adapter device.

6. The method of claim 3

wherein the step of downloading said operation programmed instructions includes the steps of:

writing a load start address of said operational programmed instructions retrieved from said non-volatile memory in a DiagRw Address register of said adapter device; and

writing said operational programmed instructions retrieved from said non-volatile memory to a DiagRw Data register of said adapter device.

7. The method of claim 3

wherein the step of downloading said data includes the steps of:

writing a load start address of said data retrieved from said non-volatile

memory in a DiagRw Address register of said adapter device; and

writing said data retrieved from said non-volatile memory to a DiagRw Data register of said adapter device.

8. The method of claim 1 further comprising the steps of:

uploading said operational programmed instructions from said volatile memory in said host adapter device to a memory in said motherboard.

9. The method of claim 8 further comprising the steps of:

detecting an occurrence of a condition that resets said host adapter device; and

downloading the previously uploaded operational programmed instructions from said memory in said motherboard to said host adapter device in response to detecting said condition.

10. A system for booting a host adapter device devoid of dedicated non-volatile program memory, wherein said host adapter device is associated with a motherboard having BIOS code stored in a non-volatile memory, said system comprising:

means for retrieving operational programmed instructions for said host adapter device from said non-volatile memory device of said motherboard;

means for downloading said operational programmed instructions from said motherboard to a volatile memory associated with said host adapter device; and

means for commencing operation of said host adapter device executing said operational programmed instructions to thereby boot said host adapter device.

11. The system of claim 10 further comprising:

means for retrieving data associated with said operational programmed instructions from said non-volatile memory device; and

means for downloading said data from said motherboard to said volatile memory.

12. The system of claim 10 further comprising:

a PCI bus coupling said host adapter device to said motherboard,

wherein the means for downloading comprises:

means for forcing said host adapter device into a diagnostic mode via said PCI bus; and

means for writing said operational programmed instructions into said volatile memory using direct memory access by said motherboard to said volatile memory via said PCI bus, and

wherein the means for commencing includes:

means for releasing said host adapter device from said diagnostic mode via said PCI bus.

13. The system of claim 12

wherein the means for forcing comprises:

means for setting a PreventIopBoot bit in a Host Diagnostic Register of said host adapter device;

means for setting a ResetAdapter bit in the Host Diagnostic Register;

means for awaiting clearing of the ResetAdapter bit in the Host Diagnostic Register; and

means for setting a DiagRwEn bit in the Host Diagnostic Register.

14. The system of claim 12 wherein the means for releasing further comprises:

means for writing an IopResetVectorRegAddr for operation of said operational programmed instructions in a DiagRw Address register of said adapter device;

means for writing an IopResetVectorValue for operation of said operational programmed instructions in a DiagRw Data register of said adapter

device;

means for clearing the PreventIopBoot bit in the Host Diagnostic Register; and

means for writing any byte value in a Write Sequence Key field in a Write Sequence register of said adapter device.

15. The system of claim 12

wherein the means for downloading said operation programmed instructions includes:

means for writing a load start address of said operational programmed instructions retrieved from said non-volatile memory in a DiagRw Address register of said adapter device; and

means for writing said operational programmed instructions retrieved from said non-volatile memory to a DiagRw Data register of said adapter device.

16. The system of claim 12

wherein the means for downloading said data includes:

means for writing a load start address of said data retrieved from said non-volatile memory in a DiagRw Address register of said adapter device; and

means for writing said data retrieved from said non-volatile memory to a DiagRw Data register of said adapter device.

17. The system of claim 10 further comprising:

means for uploading said operational programmed instructions from said volatile memory in said host adapter device to a memory in said motherboard.

18. The system of claim 17 further comprising:

means for detecting an occurrence of a condition that resets said host adapter device; and

means for downloading the previously uploaded operational programmed instructions from said memory in said motherboard to said host adapter device in

response to detecting said condition.

19. A system comprising:

a motherboard including a general-purpose processor;

a nonvolatile memory associated with said motherboard for storing BIOS code to be fetched and executed by said genera-purpose processor;

a host adapter device coupled to said motherboard wherein said host adapter device is devoid of nonvolatile memory used to store operational programmed instructions for processing by said host adapter device;

operational programmed instructions stored in said nonvolatile memory and used to operate said host adapter device; and

a downloader operable on said motherboard to retrieve said operational programmed instructions from said nonvolatile memory and to download the retrieved operational programmed instructions to said host adapter device.

20. The system of claim 19 further comprising:

a PCI bus coupling said motherboard to said host adapter device.

21. The system of claim 20 wherein said host adapter device is integral with said motherboard.

22. The system of claim 20 wherein said host adapter is a printed circuit board distinct from said motherboard.